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㉒ Received signal processing apparatus.

㉓ An apparatus for processing a digital signal which is transmitted from a transmit station by a radio equipment and contains the same repetitive information employs the principle of decision by majority. A particular signal pattern with the least error rate is determined by majority. Noncoincident bits between the determined signal pattern and each of the repeatedly received patterns are counted and, then, the number of noncoincident bits is determined on each of a predetermined number of patterns which are selected by a selector out of the repeatedly received ones. When the number is smaller than a predetermined one, the pattern is allowed for processing. That is, the signal pattern is processed by measuring the bit error rate in a transmission path with the signal pattern equivalently used as a reference.

Fig. 1A

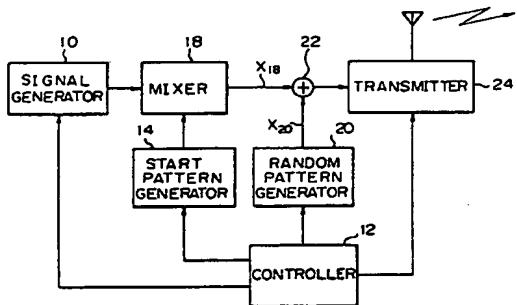
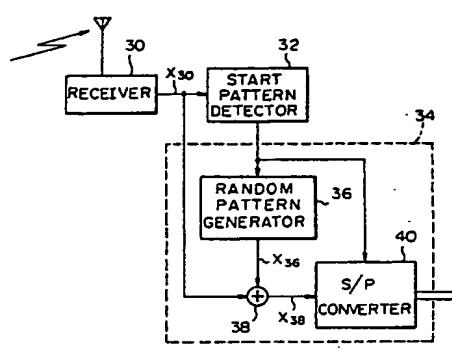


Fig. 1B-1

Fig. 1B
Fig. 1B-1 Fig. 1B-2



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RECEIVED SIGNAL PROCESSING APPARATUS

BACKGROUND OF THE INVENTION

The present invention relates to a received signal processing apparatus for processing with a majority principle a repetitive digital signal which is transmitted from a transmit station by radio equipment and representative of the same information.

In communications art, there is known an error correction system in which while a transmit station transmits the same information repeatedly, a receive station corrects errors on a decision-by-majority basis so as to enhance reliability of information. This kind of system is simpler than the other known error correction systems and extensively used. In the system employing the majority principle, how to detect errors is the important problem. Some approaches have heretofore been proposed for the detection of errors, e.g., one which determines whether the same pattern repeatedly occurs and, if it does, processes a received signal as a correct signal, and one which determines a field intensity of a received signal and, if it is at a sufficient level, processes it on a majority basis to determine the transmission quality of the signal.

The problem with the repetitive pattern scheme is that where the error probability is very high such as where the bit error rate is 10^{-2} or higher, and where a single information pattern has 50 to 100 bits, for example, the probability that the received signal is decided correct is sharply reduced and, instead, the probability that no signal is detected, i.e., the non-detection probability is increased. On the other hand, the field intensity scheme fails to provide satisfactory information on the deterioration of signals partly because upon appearance of an interference wave the system decides that the field intensity is sufficient and, therefore, fails to detect an error which actually exists in a signal, and partly because depending upon temperature and other ambient conditions the measured field intensity information and the bit error rate of received signal do not always constantly correspond to each other.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a received signal processing apparatus which despite the decision-by-majority principle achieves a considerably high error detection probability.

It is another object of the present invention to provide a generally improved received signal processing apparatus.

In one aspect of the present invention, there is provided an apparatus for processing a digital received signal in which same information appears repeatedly, comprising a start pattern detector for detecting a start pattern which precedes M repetitive information patterns which are transmitted, an information pattern receive circuit for receiving the M information patterns timed to detection of the start pattern by the start pattern detector, a store for storing the M information patterns which are received by the information pattern receive circuit a majority decision circuit for applying majority decision to the M information patterns, which are stored in the store, on a basis of bits which represent same information so as to determine a single pattern, a noncoincidence adder for determining noncoincident bits between the pattern decided by the majority decision circuit and each of the M information patterns stored in the store and, then, adding the noncoincident bits, a decision circuit for determining that the pattern decided by the majority decision circuit is acceptable for processing

when a result of summation by the noncoincidence adder is smaller than a predetermined reference value, and a signal processor for processing the pattern decided by the majority decision circuit when the decision circuit has decided that the pattern is acceptable.

In another aspect of the present invention, there is provided an apparatus for processing a digital received signal in which same information appears repeatedly, comprising a start pattern detector for detecting a start pattern which precedes a signal sequence in which M same information patterns appear repeatedly, the signal sequence being transmitted L consecutive times, an information pattern receive circuit for receiving the M information patterns timed to detection of a start pattern by the start pattern detector, a store for storing the M information patterns which are received by the information pattern receive circuit, a first majority decision circuit for applying majority decision to the M information patterns, which are stored in the store, on a basis of bits which are representative of same information so as to decide a single pattern, a first noncoincidence adder for determining noncoincident bits between the pattern decided by the first majority decision circuit and each of the M information patterns stored in the store and, then, adding the numbers of noncoincident bits, a selector for selecting out of the signal sequences, each of which comprises the M information patterns, those in which a sum of the noncoincident bits is smaller than a predetermined reference value, a second majority decision circuit for applying majority decision to all the M X N information patterns contained in N signal sequences which are selected by the selector so as to decide a single pattern, a second noncoincidence adder for determining noncoincident bits between the result provided by the second majority decision circuit and each of the M X N information patterns which are selected by the selector and then adding the numbers of noncoincident bits, a decision circuit for deciding that the pattern decided by the second majority decision circuit acceptable for processing when a sum of the noncoincident bits provided by the second noncoincidence adder is smaller than a predetermined value ρ (N) which is determined by the N, and a signal processor for processing the pattern decided by the second majority decision circuit when the decision circuit has determined that the pattern is acceptable.

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description taken with the accompanying drawings.

50 BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B are block diagrams showing a first embodiment of the received signal processing apparatus of the present invention;

Fig. 2 shows formats of signals which appear in various sections of the circuitries shown in Figs. 1A and 1B;

Figs. 3A and 3B are block diagrams showing a second embodiment of the present invention; and

Fig. 4 shows formats of signals which appear in various sections of the circuitries shown in Figs. 3A and 3B.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

While the received signal processing apparatus of the present invention is susceptible of numerous physical embodiments, depending upon the environment and requirements of use, substantial numbers of the herein shown and described embodiments have been made, tested and used, and all have performed in an eminently satisfactory manner.

Referring to Figs. 1A and 1B, a received signal processing apparatus representative of a first embodiment of the present invention is shown. Fig. 1A is a block diagram showing a transmit station which produces a predetermined digital signal, while Fig. 1B is a block diagram showing a receive station which receives the digital signal.

As shown in Fig. 1A, the transmit station includes a signal generator 10 adapted to generate an information pattern having K bits, i.e. $A = a^1 a^2 \dots a^K$. Controlled by a controller 12, the signal generator 10 delivers M (equal to or greater than 2) consecutive patterns A. A start pattern generator 14, which is also controlled by the controller 12, produces before the information patterns AA...A a fixed start pattern ST having R bits, i.e. $ST = S^1 S^2 \dots S^R$. The outputs of the signal generator 10 and start pattern generator 14 are mixed by a mixer 18 to become an information signal stream X_{1s} , in which the start pattern ST precedes the information patterns AA...A as shown in Fig. 2.

A random pattern generator 20, which is also controlled by the controller 12, generates random numbers X_{2s} which are added to the information signal stream X_{1s} by an adder 22. The output of the adder 22 is applied to a transmitter 24 to be sent to the receive station. The reason why the random numbers X_{2s} are added to the information signal stream X_{1s} is that since the signal stream X_{1s} is a

sequence of the same repetitive pattern A, applying it directly to the transmitter 24 would adversely affect the modulation characteristic due to periodic fluctuation of the frequency component. Thus, the random numbers X_{2s} are added to the repetitive patterns AA...A. The controller 12, as described, controls the timing of signal generation by the signal generator 10, that of generation of start patterns by the start pattern generator 14, that of generation of random numbers by the random pattern generator 20, and transmission by the transmitter 24.

Referring to Fig. 1B, the receive station includes a receiver 30 which applies a received signal X_{rs} to a start pattern detector 32. After the detector 32 has detected a start pattern ST, information pattern receive means 34 receives information patterns which follow the start pattern ST. The information pattern receive means 34 comprises a random pattern generator 36 adapted to generate the same random numbers X_{rs} as the random numbers X_{2s} , an adder 38, and a serial-to-parallel (SP) converter 40. The adder 38 adds the output X_{rs} of the random pattern generator 36 to that X_{rs} of the receiver 30 so as to recover a signal stream which corresponds to the signal stream X_{1s} prepared at the transmit station. The serial recovered signal stream is transformed into parallel information by the SP converter 40 in order to facilitate the subsequent processing.

The information signal stream outputted by the adder 38 will be described in detail. As shown in Fig. 2, the start pattern ST and the M information patterns AA...A prepared at the transmit station will be received by the receive station as a different pattern ST, A_1, A_2, \dots, A_M due to errors which are attributable to noise occurring in the transmission path. In Fig. 2, ST, and A_m are represented by:

$$ST_1 = S^1 S^2 \dots S^R_1$$

$$A_m = a^1_m a^2_m \dots a^K_m \quad (m = 1, 2, \dots, M)$$

If each pattern in the transmission path is free from error, all the bits are

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$$S^1 S^2 \dots S^R_1 = S^1 S^2 \dots S^R$$

$$a^1_1 a^2_1 \dots a^K_1 = a^1_2 a^2_2 \dots a^K_2 \quad (m = 1, 2, \dots, M)$$

Hence,

$$ST_1 = ST$$

$$A_m = A \quad (m = x, 1, \dots, M)$$

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The parallel outputs of the information pattern receive means 34 are stored in a store 42 as A_1, A_2, \dots, A_M . The data stored in the store 42 are read out and applied to a majority circuit 44 which then checks the bits of the patterns A_1, A_2, \dots, A_M each representative of the same information and, by majority, besides a single pattern $D = d^1 d^2 \dots d^K$. For example, d^K is the result of checking $a_1^K, a_2^K, \dots, a_M^K$ for majority; if the number of ONEs is greater than that of ZEROs, $d_K = \text{ONE}$.

The quality of the pattern D as shown in Fig. 2 is measured by a noncoincidence adder 46. Specifically, assuming that the number of noncoincident bits of the pattern D and pattern A_m is e_m ($m = 1, 2, \dots, M$), the noncoincidence adder 46 performs the following calculation as shown in Fig. 2:

$$E = e_1 + e_2 + e_M$$

It will be seen that the greater the sum E is, the greater the error rate in the transmission path and, therefore, the poorer the quality of the pattern D is. A decision circuit 48 determines whether the output E of the noncoincidence adder 46 is smaller than a predetermined reference value ρ . If the result of decision is $E < \rho$, then signal processor means 50 is allowed to process the received signal regarding the pattern D acceptable.

The signal processor means 50 includes a parity check circuit 52 which serves to check the pattern which has been decided by the majority circuit 44. Specifically, the information pattern A generated at the transmit station includes parity check bits so that the receive station may perform parity check on the result of decision D . Hence, when determined normal by the parity check circuit 52 and decided acceptable by the decision circuit 48, the pattern D is ready to be processed by the signal processor 54. Since the error rate of each bit which constitutes the pattern D is low, the effect of the parity check is considerable.

In summary, the system in the illustrative embodiment is constructed to determine a signal pattern D having the lowest error rate by decision by majority, count those bits which are noncoincident with those of the repetitively received patterns A_1, A_2, \dots, A_M , and allow the signal pattern D to be processed when the sum is smaller than a predetermined value. Stated another way, the system processes D after measuring the bit error rate of a transmission path with D equivalently used as a reference. The advantage attainable with such a system is that the bit error rate can be measured more accurately as the number of bits of the pattern A increases.

Referring to Figs. 3A and 3B, a second embodiment of the present invention is shown. Fig. 3A shows a transmit station which sends a predetermined digital signal, while Fig. 3B shows a transmit station which receives the digital signal.

As shown in Fig. 3B, the transmit station includes a signal generator 60 and a start pattern generator 62 both of which are controlled by a controller 64. As the controller 64 applies a single information transmit command to each of the signal generator 60 and the start pattern generator 62, the generator 62 generates an R bits of fixed start pattern $T = S^1 S^2 \dots S^R$ and, then, the generator 60 repeatedly gen-

erates a K bits of information pattern $A = a^1 a^2 \dots a^K$ M times (equal to or greater than 1). Hence, when L (equal to or greater than 2) information transmit commands have appeared consecutively within one transmit section, the above operation occurs L consecutive times transmitting $L \times M$ information patterns in total. A mixer 64 mixes the outputs of the signal generator 60 and start pattern generator 62 to produce an information signal stream X_{ss} as shown in Fig. 4. As will be noted, the pattern sequences STAA ... A and STAA ... A are not always continuous so that the intervals may be used for other information.

Controlled by the controller 64, a random pattern generator 66 produces random numbers X_{ss} . An adder 68 adds the random numbers X_{ss} to the information signal stream X_{ss} to provide an information sequence X_{ss} . A mixer mixes the information sequence X_{ss} with an output X_{ss} of another information signal source 70, applying the resulting information to a transmitter 74. Why the random numbers are used will not be described for such has already been described in relation to the first embodiment.

As stated above, the controller controls the operation timings of the random number generator 66 and signal source 70 and the transmission from the transmitter 74 in addition to the operations of the signal generator 60 and start pattern generator 62.

As shown in Fig. 3B, the receive station includes a receiver 80 which receives a signal X_{ss} . The following description will concentrate to processing of the start pattern ST and signal stream AA ... A which are contained in the received signal X_{ss} . In this particular embodiment, another signal processing arrangement, not shown, is assigned to the processing of a signal which is outputted by the another information signal source 70. A start pattern detector 82 detects the start pattern ST out of the received signal X_{ss} . Timed to the detection of the start pattern ST, information pattern receive means 84 receives the information patterns which follow the start pattern ST. As shown, the information pattern receive means 84 comprises a random pattern generator 86 adapted to generate the same random numbers X_{ss} as the random numbers X_{ss} , an adder 88, and a SP converter 90. Random numbers are added to the output X_{ss} of the receiver 80 to recover a signal stream which corresponds to an information signal stream X_{ss} which was prepared at the transmit station. The SP converter 90 serves to transform the serial summation output to parallel information in order to facilitate the subsequent processing.

The recovered information signal sequence X_{ss} outputted by the adder 88 will be described in detail. As shown in Fig. 4, in the signal stream X_{ss} , the start pattern ST and the M information patterns AA ... A transmitted from the transmit station are replaced with other patterns $ST_j A_{1j} A_{2j} \dots A_{Mj}$ due to noise which is involved in the transmission path. Here, j is representative of the order of the signal stream which is received in a single communication section. It will be noted that the maximum value J of j 's is not always equal to the number L of transmissions from the transmit station because the receive station may fail to detect a start pattern due to noise or accidentally detect a start pattern from another information section.

In Fig. 4, the start pattern ST_j and the information patterns A_{mj} are each represented on a bit basis as follows:

$$ST_j = S_j^1 S_j^2 \dots S_j^R \quad (j = 1, 2, \dots, J)$$

$$A_{mj} = a_{mj}^1 a_{mj}^2 \dots a_{mj}^k \quad (m = 1, 2, \dots, M) \quad (j = 1, 2, \dots, J)$$

So long as all the patterns are free from errors in the transmission path and misdetection of start patterns, their bits are maintained as:

$$S_j^1 S_j^2 \dots S_j^R = S^1 S^2 \dots S^R \quad (j = 1, 2, \dots, J; J = L)$$

$$a_{mj}^1 a_{mj}^2 \dots a_{mj}^k = a^1 a^2 \dots a^k \quad (m = 1, 2, \dots, M; j = 1, 2, \dots, J; J = L)$$

Hence,

$$ST_j = ST \quad (j = 1, 2, \dots, J; J = L)$$

$$A_{mj} = A \quad (m = 1, 2, \dots, M; j = 1, 2, \dots, J; J = L)$$

The parallel outputs of the SP converter 90 of the information pattern receive means 84 are stored in a store 92. Eventually, the store 92 stores the signal stream made up of M patterns J times as shown below:

$$\begin{array}{c} A_{11} \ A_{21} \ \dots \ A_{M1} \\ A_{12} \ A_{22} \ \dots \ A_{M2} \\ \vdots \ \vdots \ \vdots \\ A_{1J} \ A_{2J} \ \dots \ A_{MJ} \end{array}$$

The patterns held in the store 92 as described above include those which have been erroneously stored despite that they are alien ones due to accidental detection of start patterns out of other information sections. In this particular embodiment, such undesired patterns are removed by the following procedure.

Specifically, a first majority circuit 94 checks the pattern sequence $A_{1j}, A_{2j}, \dots, A_{Mj}$, which is the "j" received sequence, for majority on the basis of bits which represent the same information, thereby deciding a single pattern $D_j = d_j^1 d_j^2 \dots d_j^k$. Here, d_j^k is the result of majority decision of $a_{1j}^k, a_{2j}^k \dots a_{Mj}^k$; if the number of ONEs is greater than that of ZEROs, then $d_j^k = 1$. Assuming that the number of noncoincident bits between the pattern D_j and the pattern A_{mj} is b_{mj} , a first noncoincidence adder 96 performs a calculation $B_j = b_{1j} + b_{2j} + \dots + b_{Mj}$ as shown in Fig. 4. If the sum B_j is smaller than a predetermined reference value α , $B_j < \alpha$, a selector 98 selects the pattern sequence $A_{1j}, A_{2j}, \dots, A_{Mj}$ regarding

that it does not represent entirely alien information. Fig. 5 shows a condition wherein N signal sequences were selected by the selector 98. Specifically, N signal sequences with little error are selected out of the J signal sequences which are stored in the store 92 with D_j used as a reference, with the result that $A'_{1n} A'_{2n} \dots A'_{Mn}$ coincides with the certain "j" $A_{1j} A_{2j} \dots A_{Mj}$.

Thereafter, a second majority circuit 100 performs decision by majority on the respective bits of the $M \times N$ patterns $A'_{1n}, A'_{2n}, \dots, A'_{Mn}, A'_{1n}, A'_{2n}, \dots, A'_{Mn}, \dots, A'_{1N}, A'_{2N}, \dots, A'_{MN}$ which represent the same information. Eventually, the majority circuit 100 produces a single pattern $D = d^1 d^2 \dots d^k$ as shown in Fig. 5. A second noncoincidence adder 102 measures the quality of the output pattern D of the second majority circuit 100. Assuming that the number of noncoincident bits between the patterns D and A'_{mn} is θ_{mn} , the second noncoincidence adder 102 performs the following equation as shown in Fig. 5:

$$E = e_{11} + e_{21} + \dots + e_{M1} + \dots + e_{1n} + e_{2n} + \dots + e_{nn} + \dots + e_{1N} + e_{2N} + \dots + e_{MN}$$

This implies that the greater the sum E, the greater the error in the transmission path and, therefore, the poorer the quality of the pattern D is.

A decision circuit 104 determines whether the output E of the second noncoincidence adder 102 is smaller than a predetermined reference value ρ (N). If $E < \rho$ (N), the pattern D is regarded qualified and ready to be processed by signal processing means 106. The reference value ρ (N) is variable depending upon the receiver N. That is, the value ρ (N) increases if the number of receivers is relatively large and decreases if otherwise. This is because the number of patterns to be subjected to majority decision decreases with N to render the measurement of E inaccurate; to enhance the reliability of D, the value ρ (N), too, should be reduced.

Meanwhile, the pattern D determined by the second majority circuit 100 is applied to a parity check circuit 108. In this connection, the information pattern A prepared at the transit station is provided with parity check bits beforehand. When determined normal by the parity check circuit 108 and acceptable by the decision circuit 104, the pattern D is processed by a signal processor 110. As in the first embodiment, since the error rate of each bit which constitutes the pattern D is low, the effect of the parity check is considerable.

In summary, the apparatus in the illustrative embodiment is constructed to determine a signal pattern D having the least error rate by decision by majority, counts noncoincident bits between the pattern D and each of $M \times N$ patterns which are selected by a selector out of repeatedly received patterns, and allows the pattern D to be processed only if the count is smaller than a reference count. That is, the system processes the pattern D by equivalently measuring a bit error rate in the transmission path with D used as a reference. The advantage attainable with such a system is that since the accuracy of bit error rate measurement increases with the number of bits in the pattern A.

In addition, since L pattern sequences are sequentially transmitted from a transmit station, the probability that any of the information signal sequences is received is high despite burst errors which possibly occur in the transmission path due to fading and other causes, thereby offering a diversity effect with respect to time. Naturally, random errors are also corrected because decision by majority is made on the selected $M \times N$ patterns.

Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof. For example, the roles of the circuits 42, 44, 46, 48, 50, 52 and 54 as enclosed by dotted lines in Fig. 1 or the circuits 92, 94, 96, 98, 100, 102, 104, 106, 108 and 110 as done so in Fig. 2 may readily be fulfilled by a microcomputer. Also, the start pattern detectors 32 and 82 and the received pattern receive means 34 and 84 may be implemented by digital circuits to promote a space-and cost-effective design.

Claims

1. An apparatus for processing a digital received signal in which same information appears repeatedly, comprising:

10 start pattern detector means for detecting a start pattern which precedes M repetitive information patterns which are transmitted;

15 information pattern receive means for receiving the M information patterns timed to detection of the start pattern by said start pattern detector means;

20 store means for storing the M information patterns which are received by said information pattern receive means;

25 majority decision means for applying majority decision to the M information patterns, which are stored in said store means, on a basis of bits which represent same information so as to determine a single pattern;

30 noncoincidence adder means for determining noncoincident bits between the pattern decided by said majority decision means and each of the M information patterns stored in the store means and, then, adding the noncoincident bits;

35 decision means for determining that the pattern decided by the majority decision means is acceptable for processing when a result of summation by the noncoincidence adder means is smaller than a predetermined reference value; and

40 2. An apparatus as claimed in claim 1, wherein the information pattern includes parity bits, the signal processor means comprising parity check means for performing parity check on the pattern which is decided by the majority decision means, and signal processor means for determining the pattern decided by the majority decision means normal and processing the pattern only when the decision means has decided that the pattern is acceptable and a result of the parity check performed by said parity check means is normal.

45 3. An apparatus for processing a digital received signal in which same information appears repeatedly, comprising:

50 start pattern detector means for detecting a start pattern which precedes a signal sequence in which M same information patterns appear repeatedly, said signal sequence being transmitted L consecutive times;

55 information pattern receive means for receiving the M information patterns timed to detection of a start pattern by said start pattern detector means;

60 store means for storing the M information patterns which are received by said information pattern receive means;

65 first majority decision means for applying majority decision to the M information patterns, which are stored in said store means, on a basis of bits which are representative of same information so as to decide a single pattern;

first noncoincidence adder means for determining noncoincident bits between the pattern decided by said first majority decision means and each of the M information patterns stored in the store means and, then, adding the numbers of noncoincident bits;

selector means for selecting out of the signal sequences, each of which comprises the M information patterns, those in which a sum of the noncoincident bits is smaller than a predetermined reference value;

second majority decision means for applying majority decision to all the M X N information patterns contained in N signal sequences which are selected by said selector means so as to decide a single pattern;

second noncoincidence adder means for determining noncoincident bits between the result provided by said second majority decision means and each of the M X N information patterns which are selected by the selector means and then adding the numbers of noncoincident bits;

decision means for deciding that the pattern decided by the

second majority decision means acceptable for processing when a sum of the noncoincident bits provided by said second noncoincidence adder means is smaller than a predetermined value p (N) which is determined by the N; and

signal processor means for processing the pattern decided by the second majority decision means when said decision means has determined that the pattern is acceptable.

4. An apparatus as claimed in claim 3, wherein the information pattern includes parity bits, the signal processor means comprising parity check means for performing parity check on the pattern which is decided by the second majority decision means, and signal processor means for determining the pattern decided by the second decision means normal and processing the pattern when the decision means has decided that the pattern is acceptable and a result of the parity check performed by said parity check means is normal.

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Fig. 1A

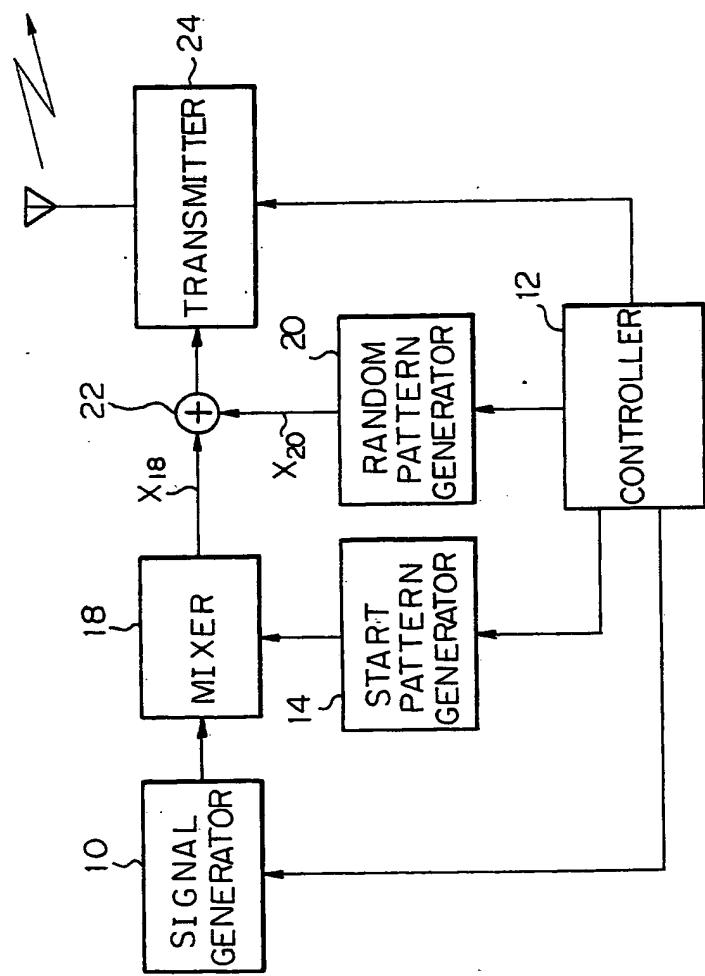


Fig.1B-1

Fig.1B

Fig.1B-1 Fig.1B-2

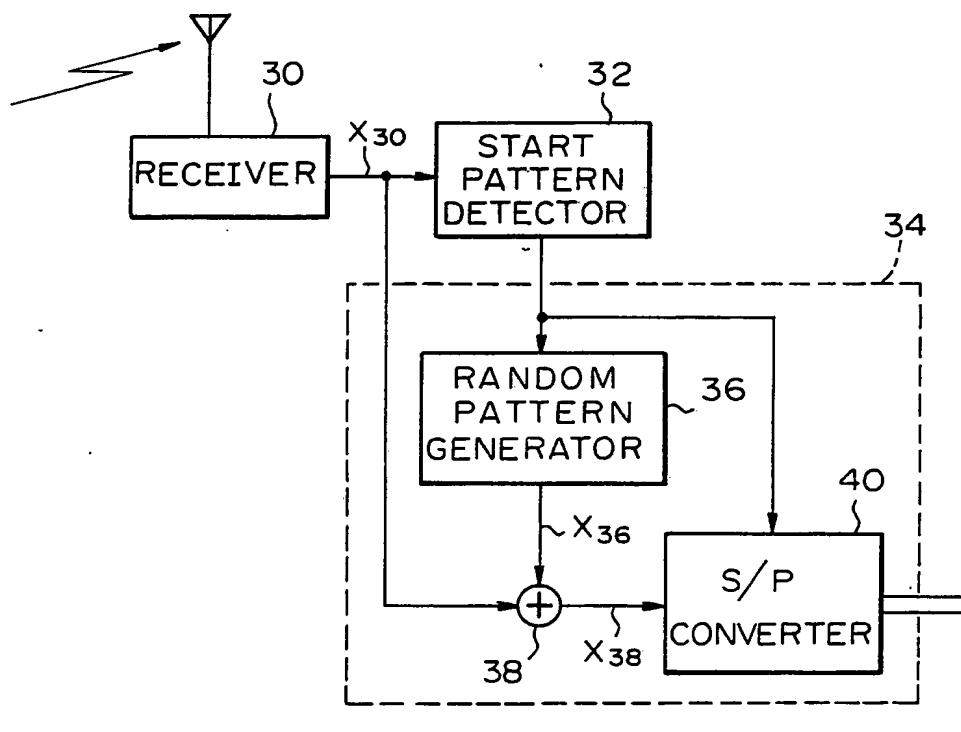


Fig. 1B-2

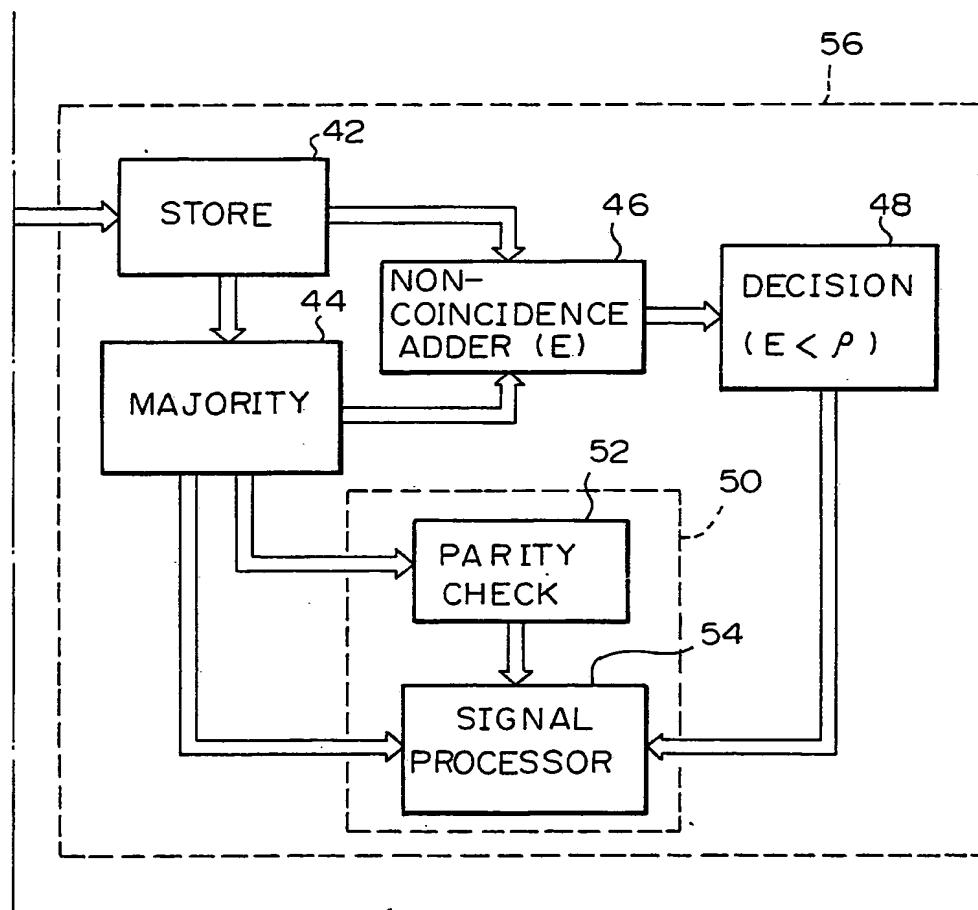


Fig. 2

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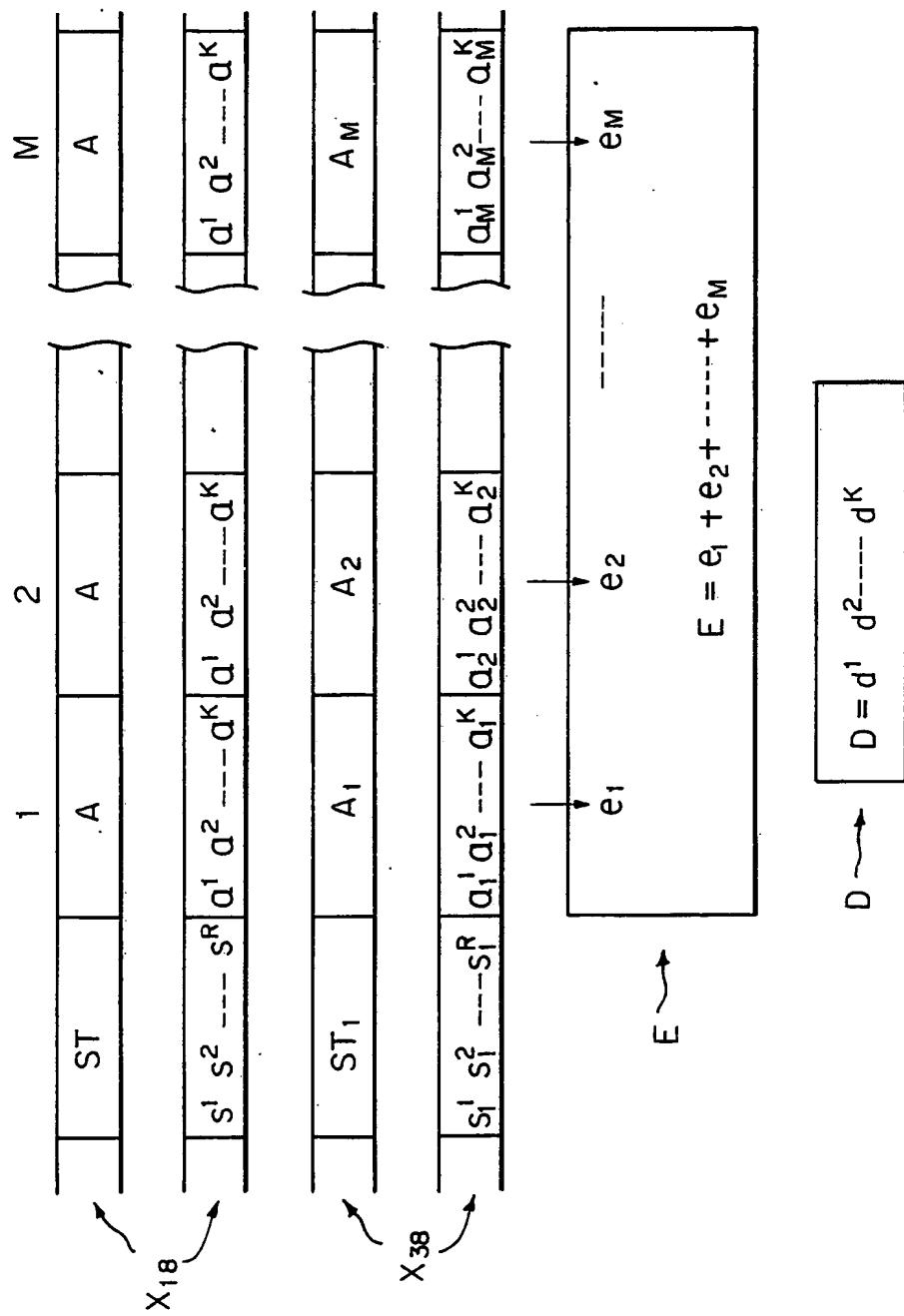


Fig. 3A

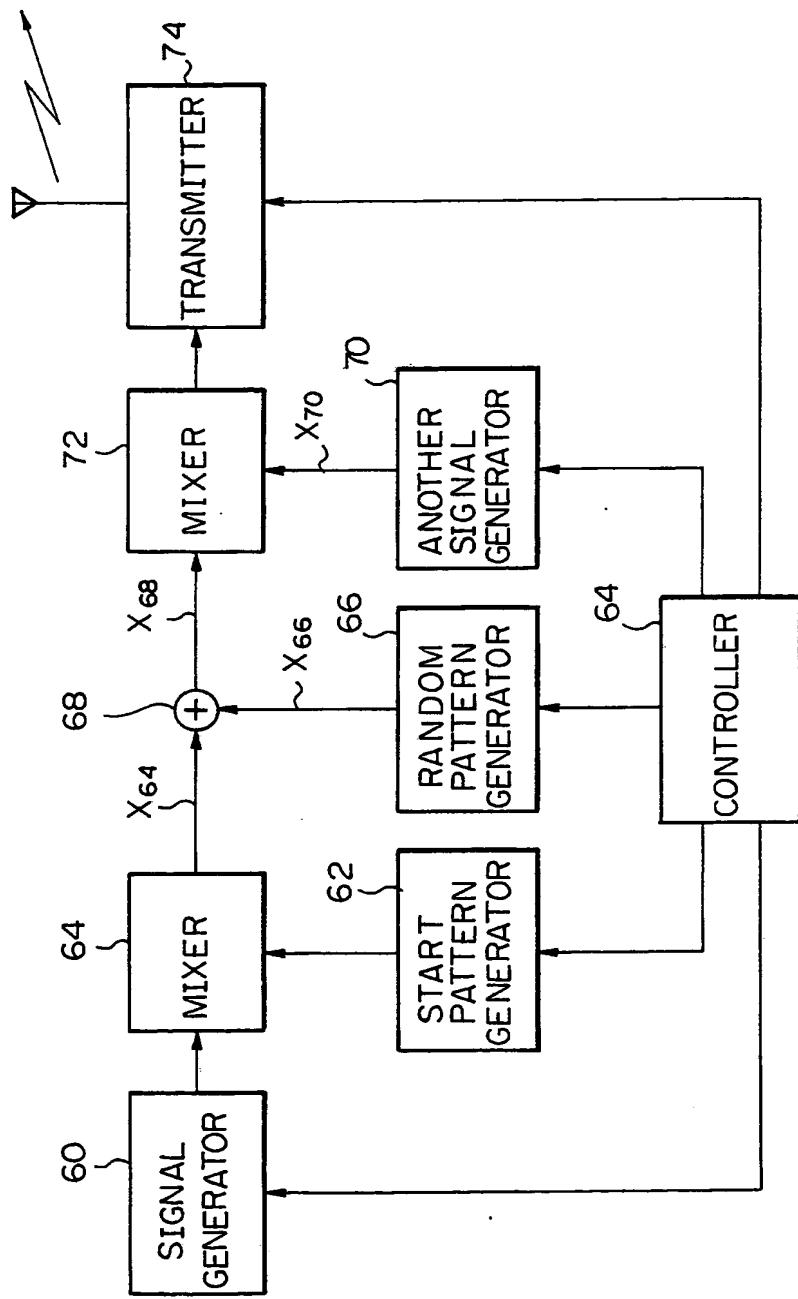


Fig. 3B-1

Fig. 3B

Fig. 3B-1 | Fig. 3B-2

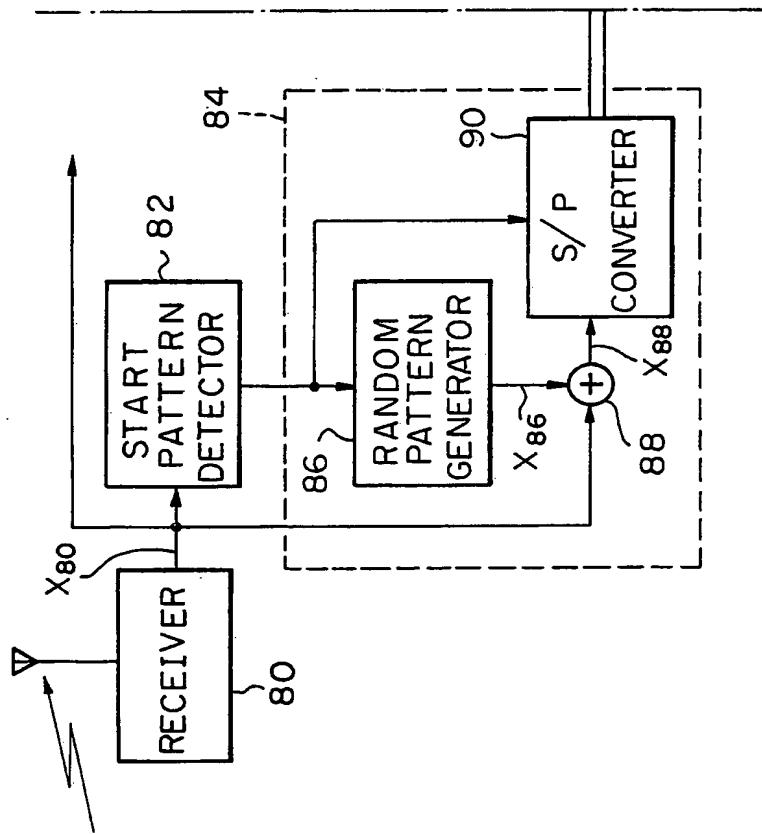


Fig. 3B-2

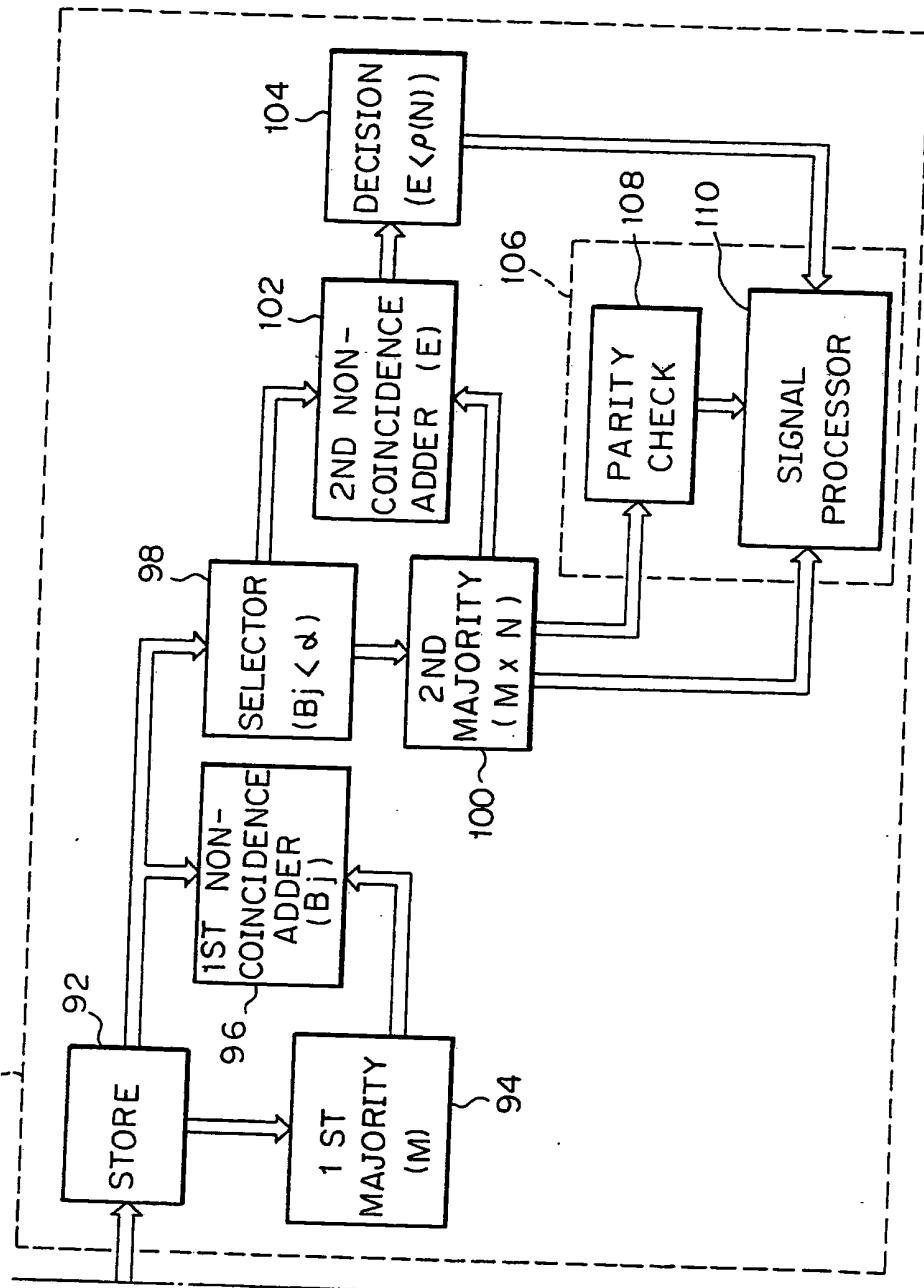


Fig. 4

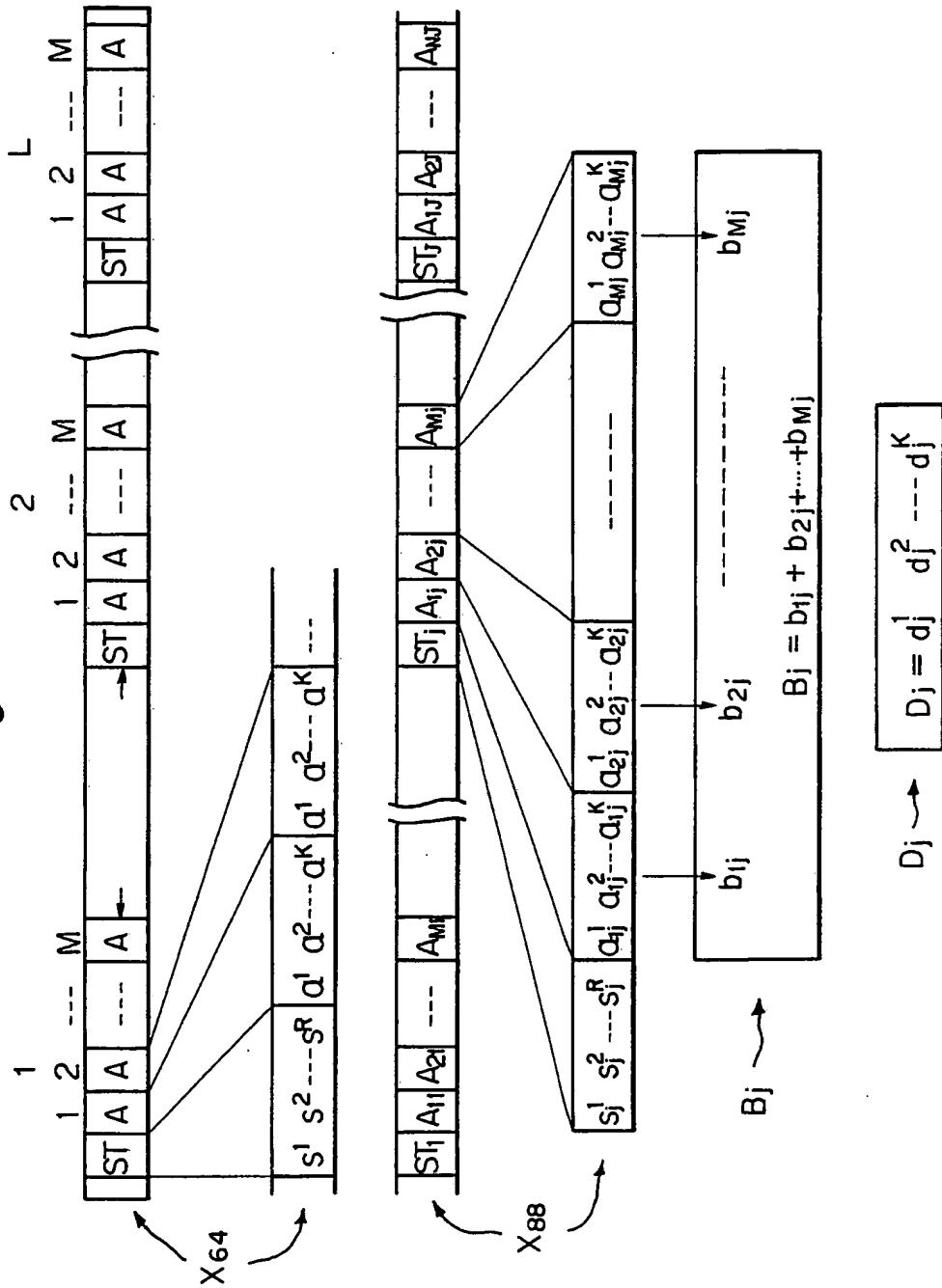
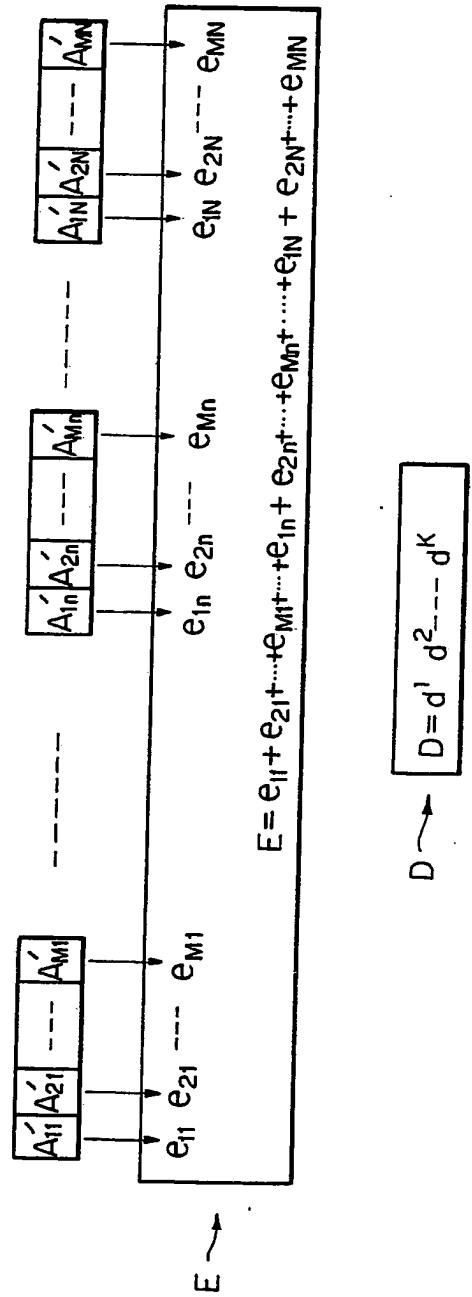


Fig. 5



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